CLAIMS

What is claimed is:

1. An iterative turbo decoder for error correcting communication signal data which recursively evaluates signal data for a selected number of iterations comprising:

a decoder data memory for storing turbo decoder estimate data generated for one decoding iteration;

a signature memory for storing a code signature corresponding to turbo decoder estimate data generated for one decoding iteration;

decoder circuitry for producing decoder estimate data for each iteration of decoding and storing it in said decoder data memory;

signature code generating circuitry for generating code signature corresponding to turbo decoder data for each decoder iteration such that each code signatures is at least twenty times smaller than the corresponding turbo decoder data; and

a comparator operatively associated with the signature code circuitry and decoder circuitry for comparing a generated code signature for turbo decoder estimate data being produced and stored for a present decoder iteration with the contents of the signature memory such that if the comparison reflects equality, the decoder circuitry ceases iteration processing and if the comparison reflects inequality, the generated code signature is stored in the signature memory where it is available for comparison relative to a code signature for a next decoder iteration.

2. An iterative turbo decoder according to claim 1 wherein said comparator is operatively associated with said decoder circuitry to cease decoder circuitry iteration processing only after a selected number of iterations have occurred and said decoder circuitry ceases iteration processing if a predetermined limit of iterations has occurred where said limit is an integer at least three greater than the selected number.

3. An iterative turbo decoder according to claim 2 wherein the selected number is four (4) and the limit is eight (8).

4. An iterative turbo decoder according to claim 1 wherein said signature code generating circuitry generates code signatures such that each code signature is at least 100 times smaller than the corresponding turbo decoder data.

5. An iterative turbo decoder according to claim 1 wherein the turbo decoder estimate data is a binary string and said signature code generating circuitry comprises a binary divider which divides corresponding binary strings of decoder data by a selected binary divisor and outputs the remainder of the division to the comparator as the code signature.

6. An iterative turbo decoder according to claim 6 wherein the decoder estimate data binary strings are at least 5,000 bits in length and the binary divisor is a 16-bit binary number whereby the code signatures are no greater than 16 bits.

7. An iterative turbo decoder according to claim 6 wherein the divisor is 1000000000000011.

8. An iterative turbo decoder according to claim 1 wherein the generated code signature is stored in the signature memory to be available for comparison relative to a code signature for a next decoder iteration by said comparator.

9. An iterative turbo decoder according to claim 1 wherein the generated code signature is stored in the signature memory to be available for comparison relative to a code signature for a next decoder iteration by said signature code generating circuitry.

10. A method for an iterative turbo decoder that error corrects communication signal data by recursively evaluating signal data for a selected number of iterations comprising:

producing decoder estimate data for each iteration of decoding and storing it in a decoder data memory;

generating code signatures corresponding to turbo decoder estimate data for each decoder iteration such that each code signature is at least twenty times smaller than the corresponding turbo decoder estimate data; and

comparing a generated code signature for turbo decoder estimate data being produced and stored for a present decoder iteration with the contents of a signature memory such that if the comparison reflects equality, iteration processing is stopped and if the comparison reflects inequality, the generated code signature is stored in the signature memory where it is available for comparison relative to a code signature for a next decoder iteration.

11. A method according to claim 10 wherein a minimum number of decoding iterations are performed before decoder iteration processing is stopped and decoder circuitry iteration processing is stopped if a predetermined limit of iterations has occurred where said limit is an integer at least three greater than the minimum number.

12. A method according to claim 11 wherein the minimum number is four (4) and the limit is eight (8).

13. A method according to claim 10 wherein the turbo decoder estimate data for each processing iteration is a binary string and the signature codes are generated by binary dividing corresponding binary strings of decoder data by a selected binary divisor and outputting the remainder of the division for comparison as the code signature.

14. A method according to claim 13 wherein the decoder estimate data binary strings are at least 5,000 bits in length and the binary divisor is a 16-bit binary number whereby the code signatures are no greater than 16 bits.

15. A method according to claim 14 wherein the divisor is 1000000000000011.

16. A method according to claim 10 wherein the generated code signature is stored in the signature memory to be available for comparison relative to a code signature for a next decoder iteration by signature code generating circuitry.